IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Jared L. Zerbe et al.

1. (MAY 0 2 2000 S

SERIAL NO.: 09/478,916

FILING DATE: January 6, 2000

TITLE: LOW LATENCY MULTI-LEVEL

COMMUNICATION

INTERFACE

Examiner: Not Yet Assigned

Art Unit: 2781

Attorney Docket No 9797-050-9 ECEIVED

MAY 0 5 2000

May 2, 2000

Group 2700

TRANSMITTAL FOR INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents Washington, DC 20231

Transmitted herewith is:

- [x] Information Disclosure Statement;
- [x] PTO 1449 Form;
- [x] copies of references listed on the PTO 1449 form; and
- [x] The Commissioner is hereby authorized to charge any fees deemed to be found to Deposit Account No. 16-1150 (9797-0050-999).

Respectfully submitted,

PENNIE & EDMONDS LLP

Date: May 2, 2000

Gary S. Williams, Reg. No. 31,066

3300 Hillview Avenue Palo Alto, CA 94304 (650) 493-4935

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INFORMATION DISCLOSURE STATEMENT ____UNDER 37 C.F.R. § 1.97

Assistant Commissioner for Patents Washington, DC 20231

Sir:

In accordance with the duty of disclosure imposed by 37 C.F.R. §§ 1.56 and 1.97 to inform the Patent Office of all references coming to the attention of Applicants or attorneys or agents for Applicants which are or may be material to the examination of the subject application, Attorneys for Applicants hereby invite the Examiner's attention to the references listed on the accompanying revised PTO Form 1449 entitled "List of References Cited".

Identification of references listed on PTO Form 1449 is not to be construed as an admission of Applicants, or attorneys for Applicants, that such references are available as "prior art" against the subject application. Consequently, Applicants respectfully decline to use form PTO-1449, since this form identifies all of the references cited therein as "Prior Art." As an alternative, Applicants submit herewith a "revised form PTO 1449" entitled "List of References Cited" instead of "List of Prior Art Cited." The right is reserved to antedate any item in accordance with standard procedure.

This submission is understood to complement the results of the Examiner's own independent search. The submission should not be construed as a representation that a search was made, or that the cited items are inclusive of all the relevant and material citations that may be available publicly.

Copies of each cited reference are enclosed. Applicants respectfully request that the Examiner review the attached references and that they be made of record in the file history of the above-captioned application.

Applicants believe that no fee is required with the submission of the enclosed List of References Cited because the Information Disclosure Statement is being filed before the mailing of the first Office Action on the merits. However, if any fee is required, the Commissioner is authorized to charge any required fee to Pennie & Edmonds LLP Deposit Account No. 16-1150 (9767-0050-999). A copy of this sheet is enclosed for accounting purposes.

Respectfully submitted,

Dated: May 2, 2000

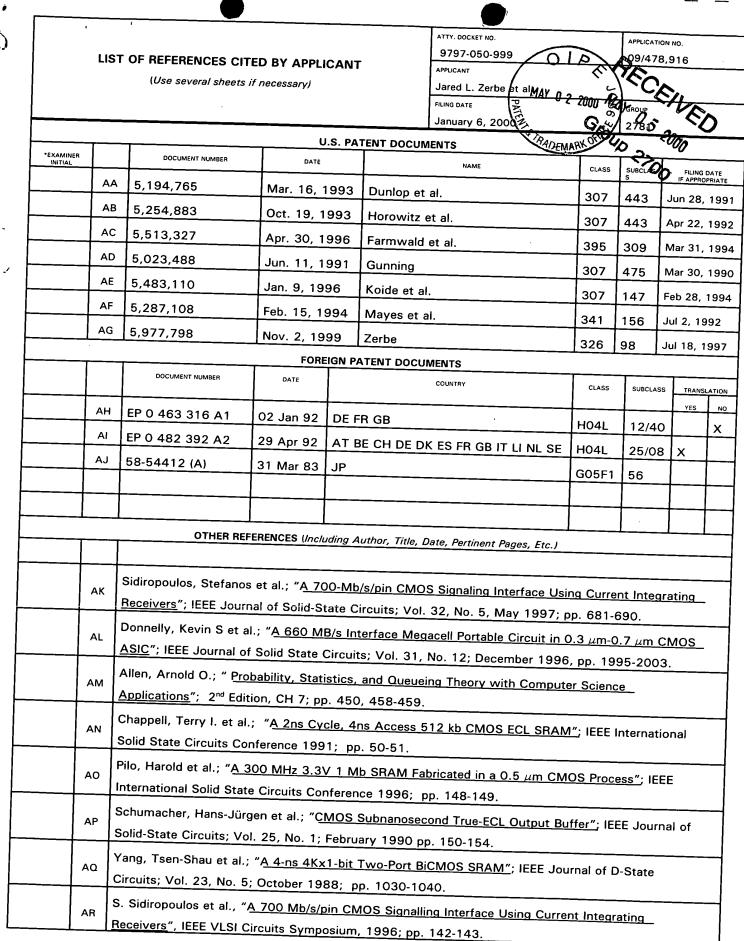
ary S. Williams

31,066 (Reg. No.)

PENNIE & EDMONDS LLP

3300 Hillview Avenue Palo Alto, CA 94304 (650) 493-4935

Enclosures



	AS	M. Bazes, "Two Novel Fully complementary Self-Biased CMOS Differential Amplifiers", IB of Solid State Circuits, Vol. 26 No. 2, February 1991.	EE Journal	
	ΑТ	of Solid State Circuits, Vol. 26 No. 2, February 1991. M. Ishibe et al., "High-Speed CMOS I/O Buffer Circuits", IEEE Journal of Solid State Grown No. 4, April 1992. J. Lee et al., "A 80ns 5v-Only Dynamic RAM", ISSCC proceedings, Paper 120, ISSCC 1	s, Vol. 27,	
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	AV	T. Seki et al., "A 6-ns 1-Mb CMOS SRAM with Latched Sense Amplifier", IEEE Journal of	5///9-	
	AW	T. Kobayashi et al., "A current-controlled latch sense amplifier and a static power-saving for low-pressure architecture", IEEE Journal of Solid State Circuits Vol. 28 No. 4., April 1		
	ΑХ	L. Tomasini et. al., "A fully differential CMOS line driver for ISDN", IEEE Journal of Solid State Circuits, Vol. 25, No. 2., April 1990.		
	AY	R. Farjad-Rad et al., "A 0.4-um CMOS 10-Gb/s 4-PAM pre-emphasis serial link transmitter", IEEE J. Solid-State Circuits, Vol. No. 34, pp. 580-585, May 1999.		
	ΑZ	E. Yeung et al., "A 2.4Gbps per pin simultaneous bidirectional parallel link with per pin skew calibration", ISSCC 2000, in press as of 1-9-2000.		
	ВА	C. Portmann et al., "A multiple vendor 2.5-V DLL for 1.6-GB/s RDRAMs", IEEE VLSI Circuits Symposium, June 1999.		
	88	A. Moncayo et al., "Bus design and analysis at 500MHz and beyond", Presented at the Design SuperCon, 1995.		
	вс	B. Lau et al., "A 2.6-Gbyte/s multipurpose chip-to-chip interface", IEEE J. Solid-State Circuits, Vol. 33, pp. 1617-1626, November 1998.		
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EXAMINER		DATE CONSIDERED THE	<i>"/</i>	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.